REMARKS/ARGUMENTS

By this paper, Claims 163-164, 168, 171, 173, 179, 181, 184, 190, 196-199, 201, 203, 205, and 208 have been amended, Claims 172, and 174-175 have been canceled, and Claims 209-210 have been added. After entry of the foregoing amendments, Claims 163-171, 173, 176-178, 179-196, and 197-210 are pending in the application, of which Claims 163, 179, and 197 are independent claims. No new matter is believed to be added herein. Entry hereof and early passage to issue are respectfully requested.

Claim Rejections – 35 USC § 103

The Office Action maintains rejection of Claims 163-208 under 35 USC § 103(a), as being unpatentable over U.S. Patent No. 6,396,148 to Eichelberger et al. ("Eichelberger") with U.S. Patent No. 5,196,377 to Wagner et al. ("Wagner") and U.S. Patent No. 6,707,124 to Wachtler et al. ("Wachtler"); or under 35 USC § 103(a) as being unpatentable over Eichelberger with Wagner and Wachtler and U.S. Patent No. 5,745,984 to Cole Jr. et al. ("Cole"); or under 35 USC § 103(a) as being unpatentable over Eichelberger with Wagner and Wachtler and further in view of U.S. Patent No. 4,866,501 to Shanefield ("Shanefield") and U.S. Patent No. 5, 541,442 to Keil et al. ("Keil"); or under 35 USC § 103(a) as being unpatentable over Eichelberger with Wagner and Wachtler, Shanefield and Keil, and further in view of Cole.

Reconsideration and withdrawal of the claim rejections are respectfully requested.

Claim 163 is directed to a chip package comprising a first insulating layer, and a die between a first portion of said first insulating layer and a second portion of said first insulating layer, wherein said die has a top surface substantially coplanar with a top surface of said first insulating layer. The chip package further comprises a second insulating layer on said top surface of said die and said top surface of said first insulating layer. The chip package further comprises a patterned metal layer over said second insulating layer, said top surface of said die and said top surface of said first insulating layer, wherein said patterned metal layer is connected to said die through an opening in said second insulating layer. The chip package further comprises a comb-shaped capacitor over said second insulating layer. The chip package further comprises a third insulating layer on said patterned metal layer and said comb-shaped capacitor,

and over said second insulating layer, said top surface of said die and said top surface of said first insulating layer.

In one aspect, therefore, the subject matter of Claim 163 includes a comb-shaped capacitor disposed over two insulating layers and a die in a chip package. Such a comb-shaped capacitor as claimed is neither taught nor suggested by the applied references.

The Office Action contends that "there are no particularly claimed 'passive' devices to structurally distinguish over the inherent capacitance/resistance/inductance properties of the overlying metallizations. There is no need to additionally 'create' a resistor, capacitor, etc. The metallizations define resistors, capacitors, and inductors. Shanefield and Keil disclose discrete passive elements as completely obvious structure in a practical application of Eichelberger." Office Action, p.3, l.19 – p.5, l.4

Applicants respectfully disagree. Even though Eichelberger's metallization structures 108 and 114 (shown in Fig. 2 of Eichelberger) may have an intrinsic capacitance, Eichelberger fails to disclose or suggest that the capacitance can be used for a capacitor. Any two metal structures (e.g., two conductive wires) possess an intrinsic capacitance therebetween. However, in order for the two metal structures to be useful as and hence considered a capacitor in a practical application, there needs to be a meaningful capacitance between the structures. In much the same way that a piece of a copper wire, even though it possesses an intrinsic resistance, cannot be useful as and considered a "resistor", two metal wires or traces that have a negligible intrinsic capacitance therebetween cannot be useful as and considered a "capacitor". Therefore, a special design consideration must be employed to create a meaningful capacitance between two metal wires to render them a "capacitor". In the claimed subject matter, for instance, the meaningful capacitance is created between metal wires 624a by fashioning the wires in a comb-shaped arrangement, as shown below in Fig. 10A of this application, to maximize the capacitance between the wires. No such special design consideration is seen to be given to any metal structures in Eichelberger. In particular, the chip package of Eichelberger is not seen to include any structure(s) that can be considered a "comb-shaped capacitor".

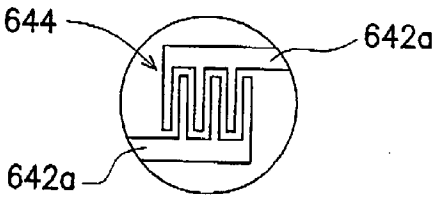

FIG. 10A

Eichelberger is not seen to disclose or suggest the claimed feature of a comb-shaped capacitor disposed over an insulating layer in a chip package.

This deficiency of Eichelberger is not seen to be remedied by any other cited references. For example, although Shanefield and Keil disclose various metal structures disposed within a chip package, neither of the references is seen to disclose or suggest any structure that can be considered a comb-shaped capacitor. The Examiner has not shown that Wagner, Wachtler, and Cole, either alone or in combination with each other or with Eichelberger, Shanefield, and Keil, disclose or suggest any structure that can be considered a comb-shaped capacitor.

At least for these reasons, Applicants respectfully submit that Claim 163 is not rendered obvious by any of the applied references and is thus allowable. Accordingly, reconsideration and withdrawal of the rejection of Claim 163 is respectfully requested.

Claim 179 is directed to a chip package comprising a first insulating layer, and a die between a first portion of said first insulating layer and a second portion of said first insulating layer, wherein said die has a top surface substantially coplanar with a top surface of said first insulating layer. The chip package further comprises a second insulating layer on said top surface of said die and on said top surface of said first insulating layer. The chip further comprises a patterned metal layer over said second insulating layer, said top surface of said die and said top surface of said first insulating layer, wherein said patterned metal layer is connected to a first metal pad of said die through a first opening in said second insulating layer, and to a

second metal pad of said die through a second opening in said second insulating layer, wherein said first metal pad is connected to said second metal pad through said patterned metal layer. The chip package further comprises a passive device over said second insulating layer.

The subject matter of Claim 179, therefore, includes a patterned metal layer disposed over a die and connecting two metal pads in the same die. Such an interconnection arrangement as claimed is neither disclosed nor suggested by the applied references.

In response to Applicants' previous response dated November 16, 2010, the Office Action contends: "Applicant argues Eichelberger teaches away from connecting two pads on the same die by a metallization layer. This argument is not convincing of patentability because the general concept of connecting pads on dies with metallizations is disclosed in Eichelberger. Any particular connections of the various pads are considered obvious given the general teachings of the applied art. There are no unobvious or unexpected results from connecting pads from the same die by a metallization. Applicant has neither disclosed nor proven any unexpected results. There is no indication in the original disclosure such arbitrary pad connection is an unexpected inventive aspect of the disclosure. Further, in an intermediate structure 3E Eichelberger discloses pads from the same die connected by a seed metallization." Office Action, p.3, ll.9-18.

Applicants respectfully disagree. Typically, an interconnection between two transistors in the same die is formed in a wafer level process, that is, formed before a die sawing process. However, in a package-level interconnection process, an interconnection is typically formed between two packaging devices, such as between a die and a substrate or between two dies, as taught in Eichelberger's Fig. 2. By contrast, the claimed subject matter provides a package-level interconnection that is formed after a die sawing process, between two metal pads in the same die. Such a package-level interconnection as claimed is not seen to be disclosed or suggested by Eichelberger. The package level interconnection as claimed produces an unexpected result of requiring less layers of fine lines in a die, which is not seen to be present in Eichelberger.

In Eichelberger's Fig. 3E, referenced by the Office Action, the seed layer 109' is seen as covering all of the top surface of a semi-finished product. Eventually, in the fabrication process associated with Eichelberger's Fig. 3G, the seed layer 109' is seen to be etched away to provide

separate remaining traces. See Eichelberger, col.8, ll.27-36. Therefore, in the final product of Eichelberger's device, Eichelberger's seed layer 109' is not shown as connecting two metal pads in the same die. Accordingly, the chip package of Eichelberger is not seen to include a structure which can be considered a patterned metal layer disposed over a die and connecting two metal pads in the same die.

The Examiner considers that "there are no particularly claimed "passive" devices to structurally distinguish over the inherent capacitance/resistance/inductance properties of the overlying metallizations. There is no need to additionally "create" a resistor, capacitor, etc. The metallizations define resistors, capacitors, and inductors. Shanefield and Keil disclose discrete passive elements as completely obvious structure in a practical application of Eichelberger." Office Action, p.3, l.19 - p.4, l.4.

Applicants respectfully disagree. Even though, in Fig. 2 of Eichelberger, the metallization structure 108 and 114 creates intrinsic resistance, capacitance and inductance, Eichelberger fails to teach, hint or suggest that the intrinsic resistance, capacitance and inductance can be used for a resistor, capacitor or inductor. It is respectfully submitted that the Examiner has focused too much on whether a metallization structure is disclosed or not, but is not giving proper consideration of the functional limitation of employing the intrinsic resistance, capacitance and inductance of the metallization structure for a resistor, capacitor or inductor. Basically, a functional limitation should be evaluated and considered, just like any other structural limitation in a claim. *See M.P.E.P. 2173.05(g).*

A functional limitation must be evaluated and considered, just like any other limitation of the claim, for what it fairly conveys to a person of ordinary skill in the pertinent art in the context in which it is used. A functional limitation is often used in association with an element, ingredient, or step of a process to define a particular capability or purpose that is served by the recited element, ingredient or step. M.P.E.P. 2173.05(g).

Accordingly, the functional limitation of a passive device is requested to be reconsidered. Furthermore, Claim 179 recites "a passive device over said second insulating layer", which

second insulation layer is disposed on a top surface of a die and on a top surface of a first insulating layer. As discussed above, the claimed subject matter provides a package-level interconnection that is formed after a die sawing process, between two metal pads in the same die. Shanefield and Keil fail to disclose or suggest that a passive device is formed in a chip package having such a package-level interconnection as claimed.

At least for these reasons, Applicants respectfully submit that Claim 179 is not rendered obvious by any of the applied references and is thus allowable. Accordingly, reconsideration and withdrawal of the rejection of Claim 179 is respectfully requested.

Claim 197 is directed to a chip package comprising a first insulating layer and a die between a first portion of said first insulating layer and a second portion of said first insulating layer, wherein said die has a top surface substantially coplanar with a top surface of said first insulating layer. The chip package further comprises a second insulating layer on said top surface of said die and on said top surface of said first insulating layer. The chip package further comprises a patterned metal layer over said second insulating layer, over said top surface of said die and said top surface of said first insulating layer, wherein said patterned metal layer comprises a ground piece connected to a first metal pad of said die through a first opening in said second insulating layer, and connected to a second metal pad of said die through a second opening in said second insulating layer, wherein said first metal pad is connected to said second metal pad through said ground piece. The chip package further comprises a passive device over said second insulating layer.

The subject matter of Claim 197, therefore, similar to the subject matter of Claim 179, includes a patterned metal layer disposed over a die and connecting two metal pads in the same die. Such an interconnection arrangement as claimed is believed to be allowable subject matter for reasons similar to the reasons set forth above with respect to Claim 179.

Furthermore, Claim 197, similar to Claim 179, also recites "a passive device over said second insulating layer", which second insulating layer is on a top surface of a die and on a top surface of a first insulating layer. This feature is also not disclosed or suggested by any of the applied references for reasons similar to the reasons set forth above with respect to Claim 179.

At least for these reasons, Applicants respectfully submit that Claim 197 is not rendered obvious by any of the applied references and is thus allowable. Accordingly, reconsideration and withdrawal of the rejection of Claim 197 is respectfully requested.

The other claims currently under consideration in the application are dependent from their respective independent claims discussed above and therefore are believed to be allowable over the applied references for at least similar reasons. Because each dependent claim is deemed to define an additional aspect of the invention, the individual consideration of each on its own merits is respectfully requested.

The absence of a reply to a specific rejection, issue, or comment does not signify agreement with or concession of that rejection, issue, or comment. In addition, because the arguments made above may not be exhaustive, there may be other reasons for patentability of any or all claims that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment or cancellation of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment or cancellation.

CONCLUSION

In view of the Amendments and Remarks herein, Applicants submit that the claims are in condition for allowance and respectfully request a notice to this effect. Should the Examiner have any questions, please call the undersigned at the phone number listed below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 502624 and please credit any excess fees to such deposit account.

Respectfully submitted,
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